AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) A Schottky diode comprising:

a semiconductor substrate;

a first metal area coupled to said semiconductor substrate;

a barrier layer coupled to said first metal area; and

a second metal area coupled to said barrier layer.

2. (Original) The Schottky diode of Claim 1 wherein said first metal area includes PtSi.

3. (Original) The Schottky diode of Claim 1 wherein said barrier layer includes SiO_2.

4. (Original) The Schottky diode of Claim 1 wherein said barrier layer includes SiN.

5. (Original) The Schottky diode of Claim 1 wherein said second metal area includes $TiSi_2$.

6. (Original) The Schottky diode of Claim 1 wherein said semiconductor substrate includes Si.

7. (Original) A Schottky diode comprising:

a semiconductor substrate;

a first metal area coupled to said semiconductor substrate; and

a second metal area coupled to said first metal.

8. (Original) The Schottky diode of Claim 7 wherein said first metal area includes PtSi.

9. (Original) The Schottky diode of Claim 7 wherein said second metal area includes $TiSi_2$.

10. (Original) The Schottky diode of Claim 7 wherein said semiconductor substrate includes Si.

11. (Original) An integrated circuit comprising:

a semiconductor substrate;

a first Schottky diode coupled to said semiconductor substrate, said first Schottky diode having a first amount of a first metal coupled to said semiconductor substrate, a first barrier layer coupled to said first amount of a first metal, and a second amount of a second metal coupled to said first barrier layer; and

a second Schottky diode coupled to said semiconductor substrate, said second Schottky diode having a third amount of said first metal coupled to said semiconductor substrate, a second barrier layer coupled to said third amount of said first metal, and a fourth amount of said second metal coupled to said second barrier layer;

wherein said first amount is at least .1% more than said third amount and said second amount is at least .1% more than said fourth amount.

12. (Original) The integrated circuit of Claim 11 wherein said first metal includes PtSi.

13. (Original) The integrated circuit of Claim 11 wherein said barrier layer includes SiO_2.

14. (Original) The integrated circuit of Claim 11 wherein said barrier layer includes SiN.

15. (Original) The integrated circuit of Claim 11 wherein said second metal includes $TiSi_2$.

16. (Original) The integrated circuit of Claim 11 wherein said semiconductor substrate includes Si.

17. (Original) An integrated circuit comprising:

a semiconductor substrate;

a first Schottky diode coupled to said semiconductor substrate, said first Schottky diode having a first amount of a first metal coupled to said semiconductor substrate and a second amount of a second metal coupled to said first amount of a first metal; and

a second Schottky diode coupled to said semiconductor substrate, said second Schottky diode having a third amount of said first metal coupled to said semiconductor substrate and a fourth amount of said second metal coupled to said third amount of said first metal;

wherein said first amount is at least .1% more than said third amount and said second amount is at least .1% more than said fourth amount.

18. (Original) The integrated circuit of Claim 17 wherein said first metal includes PtSi.

19. (Original) The integrated circuit of Claim 17 wherein said second metal includes $TiSi_2$.

20. (Original) The integrated circuit of Claim 17 wherein said semiconductor substrate includes Si.

21. (Withdrawn) A method of manufacturing a Schottky diode comprising:

providing a semiconductor substrate;

forming a barrier layer over said semiconductor substrate;

forming a first metal layer over said semiconductor substrate;

annealing said semiconductor substrate to form areas of reacted first metal and areas of un-reacted first metal;

removing selected areas of said un-reacted first metal;

forming a second metal layer over said semiconductor substrate; and

annealing said semiconductor substrate to form areas of reacted second metal and areas of un-reacted second metal.

22. (Withdrawn) The method of Claim 21 further comprising a step of forming a contact coupled to said areas of un-reacted second metal.

23. (Withdrawn) The method of Claim 21 further comprising a step of removing selected areas of said un-reacted second metal.

24. (Withdrawn) The method of Claim 21 further comprising a step of annealing said semiconductor substrate following said step of removing selected areas of un-reacted first metal.

25. (Withdrawn) A method of manufacturing a Schottky diode comprising:

providing a semiconductor substrate;

forming a first metal layer over said semiconductor substrate;

annealing said semiconductor substrate to form areas of reacted first metal and areas of un-reacted first metal;

removing selected areas of said un-reacted first metal;

forming a second metal layer over said semiconductor substrate; and

annealing said semiconductor substrate to form areas of reacted second metal and areas of un-reacted second metal.

26. (Withdrawn) The method of Claim 25 further comprising a step of forming a contact coupled to said areas of un-reacted second metal.

27. (Withdrawn) The method of Claim 25 further comprising a step of removing selected areas of said un-reacted second metal.

28. (Withdrawn) The method of Claim 25 further comprising a step of annealing said semiconductor substrate following said step of removing selected areas of un-reacted first metal.

29. (Withdrawn) A method of manufacturing an integrated circuit comprising:

providing a semiconductor substrate; and

forming at least a first Schottky diode and a second Schottky diode, said method of forming said first Schottky diode and said second Schottky diode comprising the following steps in the sequence set forth:

forming a barrier layer over said semiconductor substrate;

forming a first patterned photoresist layer over said semiconductor substrate, said first patterned photoresist layer exposing different portions of a first Schottky diode and a second Schottky diode locations;

forming a first metal layer over said semiconductor substrate;

removing said first patterned photoresist layer;

annealing said semiconductor substrate to form areas of reacted first metal and areas of un-reacted first metal;

removing selected areas of said un-reacted first metal;

forming a second patterned photoresist layer over said semiconductor substrate, said second patterned photoresist layer exposing different portions of said first Schottky diode and said second Schottky diode locations;

forming a second metal layer over said semiconductor substrate;

removing said second patterned photoresist layer; and

annealing said semiconductor substrate to form areas of reacted second metal and areas of un-reacted second metal.

30. (Withdrawn) The method of Claim 29 further comprising the step of removing selected areas of said un-reacted second metal.

31. (Currently Amended) A integrated circuit, including a first dual metal Schottky diode having a voltage drop more than .1% different than a voltage drop of a second dual metal Schottky diode, manufactured in accordance with the method of Claim 29.

32. (Withdrawn) A method of manufacturing an integrated circuit comprising:

providing a semiconductor substrate; and

forming at least a first Schottky diode and a second Schottky diode, said method of forming said first Schottky diode and said second Schottky diode comprising the following steps in the sequence set forth:

forming a first patterned photoresist layer over said semiconductor substrate, said first patterned photoresist layer exposing different portions of a first Schottky diode and a second Schottky diode locations;

forming a first metal layer over said semiconductor substrate;

removing said first patterned photoresist layer;

annealing said semiconductor substrate to form areas of reacted first metal and areas of un-reacted first metal;

removing selected areas of said un-reacted first metal;

forming a second patterned photoresist layer over said semiconductor substrate, said second patterned photoresist layer exposing different portions of said first Schottky diode and said second Schottky diode locations;

forming a second metal layer over said semiconductor substrate;

removing said second patterned photoresist layer; and

annealing said semiconductor substrate to form areas of reacted second metal and areas of un-reacted second metal.

33. (Withdrawn) The method of Claim 32 further comprising the step of removing selected areas of said un-reacted second metal.

34. (Withdrawn) A integrated circuit, including a first Schottky diode having a voltage drop more than .1% different than a voltage drop of a second Schottky diode, manufactured in accordance with the method of Claim 32.

35. (New) The Schottky diode of Claim 1 wherein said first metal area includes islands comprised of said first metal.

36. (New) The Schottky diode of Claim 7 wherein said first metal area includes islands comprised of said first metal.